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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,153	12/10/2003	Donald E. Steiss	22347-08260 (8116)	7373

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EXAMINER	
TREAT, WILLIAM M	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,153	STEISS ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 11-68* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/04, 9/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-68 are presented for examination.

2. When finding art for the elected invention, the examiner saw that the art found encompassed the non-elected invention so the examiner has withdrawn the restriction and applied art to the claims, as appropriate.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 20 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Regnier et al. (ETA: Experience ...).

5. Claims 21-26, 28, 30, 32, 34, 38, 52, and 66-68 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Rohlman et al. (Publication No. 20010032307).

6. Rohlman taught the invention of exemplary claim 21 including a network processor having a multithreaded pipeline, comprising: an upper pipeline, having an input coupled to receive a signal indicative of an instruction queue depth corresponding to a plurality of threads, the upper pipeline determining an instruction fetch sequence for the plurality of threads based on the instruction queue depth signal (paragraph [0055], Fig. 4); and a lower pipeline, comprising a first input to receive decoded instructions and

a second input to receive a thread conditions signal, the lower pipeline determining a thread execution sequence based on the thread conditions signal, the thread conditions signal indicative of an execution stall corresponding to the plurality of threads (paragraph [0054], Fig. 4). Note that the examiner has attached little significance to the term, "network processor", which he views as being defined by the limitations set forth in applicants' claim 21. However, Rohlman specifically discusses his invention in relation to modem microprocessors (paragraph [0002]), When one searches the USPAT database with combinations of the terms, modem(s) or microprocessor(s), in the same sentence as the terms, network(s) or internet, one finds over 42,000 issued patents. Inherently, Rohlman's invention qualifies as a network processor, to the extent claimed by applicants.

7. As to claim 22, Rohlman taught the network processor of claim 21, wherein the lower pipeline determines the thread execution sequence independent of the instruction fetch sequence (paragraph [0018]).

8. As to claim 23, Rohlman taught the network processor of claim 21, wherein the thread execution sequence comprises a sequence of instructions that are resequenced relative to the instruction fetch sequence (paragraph [0018]).

9. As to claim 24, Rohlman taught the network processor of claim 21, wherein the upper pipeline comprises an instruction unit to fetch the instructions (paragraphs [0016], [0017], and [0018]).

10. As to claim 25, Rohlman taught the network processor of claim 21, wherein the upper pipeline comprises a decode unit to decode the instructions (paragraphs [0016], [0017], and [0018]).

11. As to claim 26, Rohlman taught the network processor of claim 25, wherein the decode unit further comprises an instruction queue, an input of the instruction queue coupled to receive the decoded instructions from an output of the decode unit, the decode unit storing decoded instructions (paragraphs [0016], [0017], and [0018]). Note that Rohlman taught in the paragraphs cited that while he has described a pipeline having a separate decode pipeline unit (120) and queue pipeline unit (130), this is merely a design choice and a configuration where the decoding and queueing are done in one pipeline unit is merely a design choice.

12. As to claim 28, Rohlman taught the network processor of claim 21, wherein the lower pipeline comprises: a thread interleaver, having an input coupled to the first input of the lower pipeline, to dispatch a decoded instruction corresponding to a thread according to the thread execution sequence (Figs. 4 and 5).

13. As to claim 30, Rohlman taught the network processor of claim 21, wherein the lower pipeline comprises an execution unit, wherein the execution switches execution from a first thread to a second thread independent of an execution stall associated with the first thread (paragraph [0050]. As explained in paragraph [0050], when a stall results from the execution of one thread's instructions, the execution unit(s) is/are fed instructions from and alternate thread. Inherently, the execution unit must then switch

from execution of instructions from the one thread to execution of instructions from the second thread.

14. As to claim 32, Rohlman taught the network processor of claim 21, wherein the lower pipeline comprises a thread interleaver directly coupled to an execution pipeline (Figs. 4 and 5).

15. As to claims 34, 38, 52, and 66-68 fail to teach or define over rejected claims 21-26, 28, 30, and 32.

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 1-2, 11-18, 26-27, 29, 31, 33, 35-37, 46-51, 53, and 61-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rohlman et al. (Publication No. 20010032307).

19. Rohlman taught the invention of claim 21 from which claims 26-27, 29, 31, and 33 depend.

20. As to claim 26, Rohlman substantially taught the network processor of claim 25, wherein the decode unit further comprises an instruction queue, an input of the instruction queue coupled to receive the decoded instructions from an output of the decode unit, the decode unit storing decoded instructions (paragraphs [0016], [0017], and [0018]). Note that Rohlman taught in the paragraphs cited that while he has described a pipeline having a separate decode pipeline unit (120) and queue pipeline unit (130), this is merely a design choice and a configuration where the decoding and queueing are done in one pipeline unit is merely a design choice. One of ordinary skill would be motivated to provide a queue to receive the decoded instructions as they are output from the decoder(s) to provide a buffer of instructions from each thread so that execution units can be kept busy by readily available instructions for which there are resources and for which there is no thread stall.

21. As to claim 27, Rohlman taught the functional equivalent of the network processor of claim 21, wherein the upper pipeline comprises: an instruction unit to fetch instructions according to the instruction fetch sequence; a decode unit, coupled to an output of the instruction unit, to decode fetched instructions, the decode unit comprising an instruction queue to store decoded instructions; and an instruction queue depth signal line, coupled to an output of the instruction queue and an input of the instruction unit, the instruction queue depth signal line to feed back an indication of an instruction queue depth (paragraph [0055]. As to the decode unit/queue, see the previous

paragraph. Note that the examiner views the trace cache and microinstruction sequencer as being components of the instruction fetcher.

22. As to claim 29, Rohlman taught the network processor of claim 28, wherein the thread interleaver determines the thread execution sequence using two-level round robin arbitration (paragraphs [0047], [0048], [0049], [0050], [0054], and [0055], and Figs. 4 and 5). Applicants fail to define what constitutes two-level round robin arbitration in claim 29. Rohlman taught at least two levels of arbitration. One level to determine which thread might have priority based on available execution resources, as taught in paragraph [0054], and one round-robin thread instruction selection level as described in Fig. 5. To the extent claimed by applicants, the examiner views that which is taught in paragraph [0054] and Fig. 5 as constituting two-level round robin arbitration.

23. As to claim 31, Rohlman taught the network processor of claim 21, wherein the lower pipeline comprises an execution unit, wherein the execution unit executes a different thread each instruction cycle (Fig. 5). The examiner takes Official Notice that the conventional pipeline design calls for each pipeline stage to execute in one clock cycle. With one execution stage one of ordinary skill would expect Rohlman's system to be executing an instruction each clock cycle or his pipeline would stall frequently at the execution stage limiting overall throughput.

24. As to claim 33, Rohlman taught the network processor of claim 21, wherein the lower pipeline determines the thread execution sequence based on a two-level round robin arbitration. (See paragraph 22, *supra*.)

25. As to claim 1, Rohlman taught a functional equivalent of claim 1 (paragraphs [0047], [0048], [0049], and [0050] and Figs. 4 and 5). While applicants have selected a different design choice as to circuitry, the functions claimed are those described in Fig. 5. As taught by Rohlman in paragraph [0023]: "One of skill in the art would understand that there are various arrangements of the micro-instruction queue 230 of the present invention to carry out these same functions."

26. As to claims 2, 11, and 16, they fail to teach or define over rejected claims 1, 21-34, 38, 52, and 66-68.

27. As to claims 12-15, these are merely conventional reasons for stalls and Rohlman taught in paragraph [0019]: "Any reference to a stall in this description includes all of the circumstances that may cause a stall." Certainly, Rohlman meant to include conventional stalls in such a statement.

28. As to claim 17, Rohlman taught an instruction conditions signal indicative of one or more thread ages (paragraph [0055].

29. As to claim 18, it fails to teach or define over rejected claims 1-2, 11-17, 21-34, 38, 52, and 66-68.

30. As to claim 19, Rohlman taught the processor of claim 16, wherein the instruction conditions signal comprises a priority indicator generated external to the selection unit to indicate a priority level of one or more threads (paragraph [0054]. Based on available resources in the execution unit, priority is given to one thread over another.

31. As to claims 35-38, 46-51, 53, and 61-65, they fail to teach or define over rejected claims 1-2, 11-19, 21-34, 38, 52, and 66-68.

32. Claims 34-43, 45, 52-58, 60 and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky et al. (Publication No. 20020062435).

33. Nemirovsky taught the invention of exemplary claim 34 including a method of thread interleaving, comprising: receiving a plurality of decoded instructions associated with a plurality of threads (paragraphs [0040] and [0041]); receiving thread conditions associated with the plurality of threads, the thread conditions indicative of an execution stall (paragraphs [0069] and [0070]); selecting a thread from the plurality of threads based on the thread conditions; and outputting a decoded instruction corresponding to the thread selection (paragraph [0042], first sentence).

34. As to claim 35, Nemirovsky taught the method of claim 34, wherein the selecting comprises selecting a thread each clock cycle (paragraph [0042], first sentence). It is the examiner's contention that the intended meaning of "cycle-by-cycle" is "clock-cycle-by-clock-cycle". Nemirovsky proposes using his system in real-time applications with stringent timing requirements (paragraph [0068]) which argues for a clock-cycle-by-clock-cycle selection of thread instructions for execution to keep his multiple functional unit pipeline fully utilized and to meet the stringent timing requirements of necessary for modern network routers and switches (paragraph [0074]).

35. As to claim 36, Nemirovsky taught the method of claim 34, further comprising: executing the decoded instruction associated with a different thread each clock cycle (paragraphs [0040] and [0041]), wherein the selecting the thread occurs each clock cycle (paragraph [0042], first sentence).

36. As to claim 37, Nemirovsky taught the method of claim 34, further comprising: executing a first decoded instruction associated with a first thread during a first clock cycle; and executing a second decoded instruction associated with a second thread during a second clock cycle, the executing the second decoded instruction independent of a thread condition associated with the first thread (paragraph [0042], first sentence, and paragraphs [0069] and [0070]).

37. As to claim 38, Nemirovsky taught the method of claim 34, further comprising: attempting to execute the selected instruction; detecting an execution stall during the attempting to execute; and generating an execution stall signal (paragraph [0066], first three sentences, and paragraphs [0069] and [0070]).

38. As to claim 39, Nemirovsky taught the method of claim 34, wherein the selecting one of the plurality of threads further comprises: selecting a thread associated with a high priority instruction from the plurality of threads; selecting a thread associated with a low priority instruction from the plurality of threads; and selecting between the high priority selection and the low priority selection (paragraphs [0036] and [0037] and the first sentence of paragraph [0042]).

39. As to claim 40, Nemirovsky taught the method of claim 39, further comprising: receiving a previous thread selection, wherein the high priority selection and the low priority selection use round robin arbitration to select a next thread (paragraph [0065], first three sentences).

40. As to claim 41, Nemirovsky taught the method of claim 39, further comprising: receiving instruction conditions indicative of availability, wherein the high priority

selection comprises selecting a thread associated with an available high priority instruction, and wherein the low priority selecting comprises selecting a thread associated with an available low priority instruction (paragraph [0069]; paragraph [0070], first sentence; paragraphs [0036] and [0037]).

41. As to claim 42, Nemirovsky taught the method of claim 39, wherein the selecting between the high priority selection and the low priority selection comprises selecting by default the high priority selection (paragraph [0061], 2nd sentence).

42. As to claim 43, Nemirovsky taught the method of claim 39, wherein the selecting between the high priority selection and the low priority selection comprises selecting the low priority selection after a predetermined number of successive high priority selections (paragraph [0061], first three sentences).

43. As to claim 45, Nemirovsky taught the method of claim 39, wherein the selecting between the high priority selection and the low priority selection comprises selecting the low priority selection if there is no high priority selection (paragraph [0061], 2nd sentence).

44. As to claim 52, Nemirovsky taught a processor, comprising: queuing means for receiving a plurality of decoded instructions associated with a plurality of threads; selection means for receiving thread conditions associated with the plurality of threads, the thread conditions indicative of an execution stall, and selecting a thread from the plurality of threads based on the thread condition; and outputting means, coupled to the queuing means and the selection means, for outputting a decoded instruction from the queuing means corresponding to the thread selection. Claim 52 differs from rejected

claims 34-43 and 45 only in its mention of a queuing means for decoded instructions of the threads which is taught by Nemirovsky (paragraph [0040]).

45. As to claims 53-58, 60 and 68, they fail to teach or define over rejected claims 34-43, 45, and 52.

46. Claims 35-51 and 53-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al. (Publication No. 20020062435).

47. As to claims 35-37 and 53, the examiner explained why one of ordinary skill would be motivated to make Nemirovsky's cycle-by-cycle interleaving clock-cycle-by-clock-cycle interleaving, etc.

48. As to claims 38-43, 45, 54-58, and 60, though Nemirovsky does not describe his system exactly as applicants have claimed, it is clear from the passages identified, *supra*, in relation to these claims that Nemirovsky's system inherently has the functionality to perform the claimed functions to the extent claimed (paragraph [0079]).

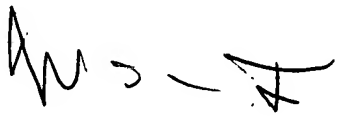
49. As to claims 38, 44, 46-51, 59, and 60-65, these are merely conventional stalls which are obvious design choices given Nemirovsky's teachings (paragraphs [0069], [0070], [0071], and claim 46),

50. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

51. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

52. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Treat



Primary Examiner